What is claimed is:

1. A power-on reset circuit comprising:

a capacitor connected between a power supply line and an internal node;

a MOS transistor having its drain connected to said internal node and its source connected to a reference potential, and set in the OFF state; and

an output portion outputting a reset signal when the potential of said internal node decreases below a threshold voltage after the application of a power supply voltage to said power supply line.

2. A power-on reset circuit according to Claim 1, wherein said capacitor is a MOS capacitor comprising a MOS transistor having its source and drain connected to said power supply line and its gate connected to said internal node.

3. A power-on reset circuit comprising:

a first capacitor connected between a power supply line and a first node;

a first MOS transistor connected between said first node and a second node, and ON/OFF controlled based on a first pulse signal;

a second MOS transistor connected between said second node and a reference potential, and ON/OFF controlled based on a second pulse signal;

a second capacitor connected between said second node and said reference potential;

a timing control unit for generating said first and second pulse signals in synchronism with a clock signal externally applied thereto; and

an output portion outputting a reset signal when the potential of said internal node decreases below a threshold voltage after the application of a power supply voltage to said power supply line.

4. A power-on reset circuit according to Claim 3, wherein said first MOS transistor is designed to be OFF when said first pulse signal is not applied thereto and to go ON with said first pulse signal applied thereto, and wherein said second MOS transistor is designed to be OFF when said second pulse signal is not applied thereto and to go ON with said second pulse signal applied thereto.

5. A power-on reset circuit according to Claim 3, wherein said timing control unit outputs said first pulse signal when the clock signal externally applied thereto is shifted from a first logical level to a second logical level, and outputs said second pulse signal when the clock signal is shifted from the second logical level to the first logical level.

6. A power-on reset circuit according to Claim 4, wherein said timing control unit outputs said first pulse signal when the clock signal externally applied thereto is shifted from a first logical level to a second logical level, and outputs said second pulse signal when the clock signal is shifted from the second logical level to the first logical

level.

7. A power-on reset circuit according to any one of Claims 3, 4, 5 and 6, wherein said first capacitor is a MOS capacitor comprising a MOS transistor having its source and drain connected to said power supply line and its gate connected to said internal node.

8. A power-on reset circuit according to any one of Claims 1 to 6, wherein said output portion has a hysteresis characteristic.

9. A power-on reset circuit according to Claim 7, wherein said output portion has a hysteresis characteristic.